REMARKS

This responds to the Office Action mailed on November 3, 2004.

Claims 10, 14, and 15 are amended. Claims 31-35 are added. As a result, claims 10-22, and 31-35 are now pending in this application.

Reservation of the Right to Swear Behind References

Applicant maintains the right to swear behind any references which are cited in a rejection under 35 U.S.C. §§102(a), 102(e), 103/102(a), and 103/102(e). Statements distinguishing the claimed subject matter over the cited references are not to be interpreted as admissions that the references are prior art.

Claim objections

Claim 15 was objected to because of the following informalities: "logic function" should be "logic circuit" in order to comply with established antecedent in claim 10. Claim 15 is amended for clarity.

§103 Rejection of the Claims

Claim 10 was rejected under 35 USC § 103(a) as being unpatentable over Taya et al. (U.S. 5,778,214), hereafter Taya, in view of Yamamoto et al. (JP Publication 06-120937), hereafter Yamamoto.

Applicant respectfully traverses because a *prima facie* case of obviousness has not been made.

Claim 10 is amended for clarity. As amended, claim 10 recites:

"a plurality of input nodes;
a plurality of output nodes;
a plurality of register circuits, each of the register circuits being connected between one of the input nodes and one of the output nodes to receive a plurality of input bits at one of the input nodes and to provide at one of the output nodes a plurality of output bits based on the plurality of input bits;
a logic circuit connected to the register circuits to perform a logic function on the plurality of input bits held by one of the register circuits among the plurality of the register circuits with the plurality of input bits held by the other register circuits among the plurality of register circuits; and

a controller to configure the register circuits based on a result from the logic function of the logic circuit to align the plurality of output bits provided by one output node with a plurality of output bits provided by other output nodes when the plurality of input bits received at one of the input nodes are misaligned with the plurality of input bits received at the other input nodes by one or more bit time intervals."

Taya teaches, in FIG. 2, a plurality of shift registers 22a, 22b, and 22c. All of the shift registers 22a, 22b, and 22c receive data from a plurality of data input nodes. FIG. 2 of Taya shows that the plurality of data input nodes are connected to the same node, which is the output nodes of switches SW 12a, 12b, 12c, and 12n. Applicant is unable to find in Taya a showing or a fair suggestion that "each" of the shift registers 22a, 22b, and 22c of Taya is connected between "one" of the input nodes and "one" of the output nodes to receive a plurality of input bits at one of the input nodes and to provide at one of the output nodes a plurality of output bits based on the plurality of input bits. In contrast, claim 10 recites "each of the register circuits being connected between one of the input nodes and one of the output nodes to receive a plurality of input bits at one of the input nodes and to provide at one of the output nodes a plurality of output bits based on the plurality of input bits".

Further, Applicant is unable to find in Taya a showing or a fair suggestion of "a logic circuit connected to the register circuits to perform a logic function on the plurality of input bits held by one of the register circuits among the plurality of the register circuits with the plurality of input bits held by the other register circuits among the plurality of register circuits", and "a controller to configure the register circuits based on a result from the logic function of the logic circuit to align the plurality of output bits provided by one output node with a plurality of output bits provided by other output nodes when the plurality of input bits received at one of the input nodes are misaligned with the plurality of input bits received at the other input nodes by one or more bit time intervals", as claimed in claim 10.

Yamamoto teaches a first shift register 1, a second shift register 2, a comparison means 3, and a control means 5. Comparison means 3 compares the content (a plurality of bits) of second shift register 2 with the content of a storage means 4. Based on the comparison result from comparison means 3, control means 5 shifts one bit from shift register 1 to shift register 2. After the shift, comparison means 3 repeats the comparison between the content (new content after the shift) of second shift register 2 with the content of storage means 4. Applicant is unable to find

in Yamamoto a showing or a fair suggestion that comparison means 3 of Yamamoto performs a logic function on the plurality of bits of first shift register 1 with the plurality of bits of second shift register 2. In contrast, claim 10 recites a logic circuit connected to the register circuits to perform a logic function on the plurality of input bits "held by one of the register circuits" among the plurality of the register circuits "with" the plurality of input bits "held by the other register circuits" among the plurality of register circuits. Moreover, Applicant is unable to find in Yamamoto a showing or a fair suggestion that the control means 5 of Yamamoto is to configure shift register 1 and shift register 2 to align the bits at the output node of shift register 1 with the bits at the output node of shift register 2. In contrast, claim 10 recites that the controller of claim 10 is to "align the plurality of output bits provided by one output node with a plurality of output bits provided by other output nodes when the plurality of input bits received at one of the input nodes are misaligned with the plurality of input bits received at the other input nodes by one or more bit time intervals".

The reasons presented above show that Applicant is unable to find in Taya and Yamamoto, alone or in combination, all of the things recited in claim 10. Further, even if Taya and Yamamoto are combined as proposed by the Office Action, there is no reasonable expectation of success to achieve the things recited in claim 10 because Taya uses a detection circuit 24 (FIG. 2) and a counter 13 for varying a delay of a variable delay circuit 11 to adjust a phase difference between a data signal and a clock signal, whereas Yamamoto uses compare means 3 and control means 5 for shifting bits from one shift register to another shift register based on a comparison result between one of the shift registers with a storage mean. Accordingly, Applicant requests that the rejection of claim 10 be reconsidered and withdrawn and that claim 10 be allowed.

Claim 11 was rejected under 35 USC § 103(a) as being unpatentable over Taya et al. and Yamamoto et al. as applied to claim 10, and further in view of Fukuoka (U.S. 6,467,063).

Claim 11 depends on independent claim 10. As presented above, claim 10 is patentable over Taya and Yamamoto. Thus, claim 11 is also patentable over Taya and Yamamoto, and further over Fukuoka for at least the reasons presented above regarding claim 10. Accordingly,

Applicant requests that the rejection of claim 11 be reconsidered and withdrawn and that claim 11 be allowed.

Claims 12-13 were rejected under 35 USC § 103(a) as being unpatentable over Fukuoka, Taya, and Yamamoto as applied to claim 11 above, and further in view of Moriwaki et al. (U.S. 6,753,872).

Claims 12 and 13 indirectly depend on independent claim 10. As presented above, claim 10 is patentable over Taya and Yamamoto. Thus, claims 12 and 13 are also patentable over Fukuoka, Taya, Yamamoto, and further over Morikawi for at least the reasons presented above regarding claim 10. Accordingly, Applicant requests that the rejection of claims 12 and 13 be reconsidered and withdrawn and that claims 12 and 13 be allowed.

Claim 15 was rejected under 35 USC § 103(a) as being unpatentable over Taya and Yamamoto as applied to claim 10 above, and further in view of Jaquette (U.S. 5,737,371).

Claim 15 depends on independent claim 10. As presented above, claim 10 is patentable over Taya and Yamamoto. Thus, claim 15 is also patentable over Taya and Yamamoto, and further over Jaquette for at least the reasons presented above regarding claim 10. Accordingly, Applicant requests that the rejection of claim 15 be reconsidered and withdrawn and that claim 15 be allowed.

Claims 18-20 were rejected under 35 USC § 103(a) as being unpatentable over Moriwaki in view of Grondalski (U.S. 6,108,763).

Applicant respectfully traverses because a *prima facie* case of obviousness has not been made.

Independent claim 18 recites, among other things, a plurality of register circuits in which "each" of the register circuits includes a shift register and a select circuit. Moriwaki shows, in FIG. 5, a data transfer circuit 12 having a plurality of register circuits 50-1 through 50-64. Applicant is unable to find in Moriwaki a showing or a fair suggestion that "each" of the register circuits 50-1 through 50-64 of Moriwaki includes a shift register and a select circuit. Moriwaki shows a selector 51 (FIG. 5). However, selector 51 is the only selector used to select all of the register circuits 50-1 through 50-64 of Moriwaki. In contrast, claim 18 recites, among other things, a plurality of register circuits in which "each" of the register circuits includes a shift register and a select circuit.

Notwithstanding that Applicant is unable to find in Moriwaki a showing or a fair suggestion that "each" of the register circuits 50-1 through 50-64 of Moriwaki includes a shift register and a select circuit, Applicant believes that the function of data transfer circuit 12 of Moriwaki would be destroyed if selector 51 of Moriwaki is connected in a way that the select circuit of claim 18 is connected as recited in claim 18. For example, claim 18 also recites that the shift register including a number of register cells and that the select circuit connected to "a subset" of the number of register cells. Moriwaki teaches that each of the register circuits 50-1 through 50-64 has a capacity of 24 bits (column 9, lines 10-11); and each of the register circuits 50-1 through 50-64 is connected to an internal data bus 55 via a 24-bit sub data bus (FIG. 5, and column 9, lines 32-33). Since each of the register circuits 50-1 through 50-64 has a capacity of 24 bits, connecting internal data bus 55 to a "subset" of 24 bits in each of register circuits 50-1 through 50-64 may reduce the total number of bits transferred from the register circuits 50-1 through 50-64 to internal data bus 55. Thus, improper data transfer may occur and the function of data transfer circuit 12 of Moriwaki would be destroyed.

The reasons presented above show that claim 18 is not obvious over Moriwaki. Claim 18 is also not obvious over proposed combination of Moriwaki and Grondalski because Applicant is also unable to find in the proposed combination of Moriwaki and Grondalski a plurality of register circuits in which "each" of the register circuits includes a shift register and a select circuit. Accordingly, Applicant requests that the rejection of claim 18 be reconsidered and withdrawn and that claim 18 and its dependent claims 19 and 20 be allowed.

Claim 19 depends on independent claim 18. As presented above, claim 18 is patentable over Moriwaki. Thus, claim 19 is also patentable over Moriwaki and Grondalski for at least the reasons presented above regarding claim 18, plus the things recited in claim 19. Accordingly, Applicant requests that the rejection of claim 19 be reconsidered and withdrawn and that claim 19 be allowed.

Claim 20 indirectly depends on independent claim 18. As presented above, claim 18 is patentable over Moriwaki. Thus, claim 20 is also patentable over Moriwaki and Grondalski for at least the reasons presented above regarding claim 18, plus the things recited in claim 20. Accordingly, Applicant requests that the rejection of claim 20 be reconsidered and withdrawn and that claim 20 be allowed.

Claim 21 was rejected under 35 USC § 103(a) as being unpatentable over Moriwaki and Grondalski as applied to claim 19 above, and further in view of Barnsely et al. (U.S. 5,430,812).

Applicant respectfully traverses because a *prima facie* case of obviousness has not been made.

Claim 21 indirectly depends on independent claim 18. As presented above, claim 18 is patentable over Moriwaki and Grondalski. Thus, claim 21 is also patentable over Moriwaki and Grondalski, and further over Barnsley for at least the reasons presented above regarding claim 18. Accordingly, Applicant requests that the rejection of claim 21 be reconsidered and withdrawn and that claim 21 be allowed.

Claim 22 was rejected under 35 USC § 103(a) as being unpatentable over Moriwaki and Grondalski as applied to claim 19 above, and further in view of Frisch et al. (U.S. 4,707,834).

Applicant respectfully traverses because a *prima facie* case of obviousness has not been made.

Claim 22 indirectly depends on independent claim 18. As presented above, claim 18 is patentable over Moriwaki and Grondalski. Thus, claim 22 is also patentable over Moriwaki and Grondalski, and further over Frisch for at least the reasons presented above regarding claim 18. Accordingly, Applicant requests that the rejection of claim 22 be reconsidered and withdrawn and that claim 22 be allowed.

Allowable Subject Matter

Claims 14 and 16-17 were objected to as being dependent upon a rejected base claim, but were indicated to be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claim 14 is rewritten only to put claim 14 in independent form. The scope of claim 14 is not narrowed. Claims 14, 16, and 17 are now in condition for allowance.

Conclusion

Applicant respectfully submits that the claims are in condition for allowance and notification to that effect is earnestly requested. The Examiner is invited to telephone Applicant's representative ((612) 373-6969) to facilitate prosecution of this application.

If necessary, please charge any additional fees or credit overpayment to Deposit Account No. 19-0743.

Respectfully submitted,

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